Please amend the claims as follows (this listing of claims replaces all prior listings):

21. (Currently amended) ~~Apparatus for providing a variable level of capacitance,~~ An apparatus comprising:

~~a plurality of~~ MOSFET capacitors, each capacitor selectable ~~through~~ by an independent control signal generated by a logic circuit, the selected capacitors ~~providing~~ to provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors; and

buffer circuitry for decoupling the ~~plurality of~~ capacitors from the logic circuit to prevent noise in the logic circuit from affecting the ~~plurality of~~ capacitors.

22. (Previously Presented) The apparatus of claim 21, further comprising a filter circuit connected to a power supply to generate a filtered power supply signal that is used to power the buffer circuitry.

23. (Currently amended) The ~~circuit~~ apparatus of claim 21, further comprising transmission gates, each of which corresponds to one of the ~~plurality of~~ capacitors and can be turned on by the independent control signal when the corresponding capacitor is selected.

24. (New) The apparatus of claim 23 in which a node of each of the transmission gates is connected to a gate node of the corresponding MOSFET capacitor.

25. (New) The apparatus of claim 22 in which the filtered power supply signal is also used to bias at least one of the MOSFET capacitors.

26. (New) The apparatus of claim 21, further comprising a filter circuit connected to a power supply to generate a filtered power supply signal to bias at least one of the MOSFET capacitors.

27. (New) The apparatus of claim 21, wherein each of a subset of one or more of the MOSFET capacitors comprises a P-type enhancement mode MOSFET.

28. (New) The apparatus of claim 27, further comprising a filter circuit connected to a power supply to generate a filtered power supply signal that is connected to the source and drain of at least one of the MOSFET capacitors.

29. (New) The apparatus of claim 21, wherein each of a subset of one or more of the MOSFET capacitors comprises an N-type depletion mode MOSFET.

30. (New) The apparatus of claim 21 in which at least one of the MOSFET capacitors has a capacitance that is less than 1 pF.

31. (New) An apparatus comprising:

~~a plurality of~~ on-chip capacitors disposed on an integrated circuit, each capacitor selectable through an independent control signal generated by a logic circuit, the selected capacitors to provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors, each capacitor comprising at least one of an on-chip metal capacitor and an on-chip poly capacitor; and

buffer circuitry for decoupling the ~~plurality of~~ capacitors from the logic circuit to prevent noise in the logic circuit from affecting the selected capacitors.

32. (New) The apparatus of claim 31, further comprising a low pass filter connected to a power supply to generate a filtered power supply signal that is used to power the buffer circuitry.

33. (New) The apparatus of claim 31, further comprising transmission gates, each of which corresponds to one of the ~~plurality of~~ capacitors and can be turned on by the independent control signal when the corresponding capacitor is selected.

34. (New) The apparatus of claim 33 in which the buffer circuitry decouples the transmission gates from the logic circuit to prevent noise in the logic circuit from affecting the selected capacitors.

35. (New) A method comprising:

selecting a subset of a plurality of MOSFET capacitors to provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors, the selecting including using a logic circuit to generate control signals to select the subset of capacitors; and

decoupling the capacitors from the logic circuit by using a buffer circuitry to prevent noise in the logic circuit from affecting the plurality of capacitors.

36. (New) The method of claim 35, further comprising generating a filtered power supply signal, by using a low pass filter, to power the buffer circuitry.

37. (New) The method of claim 36, further comprising biasing at least one of the MOSFET capacitors using the filtered power supply signal.

38. (New) The method of claim 35, further comprising generating a filtered power supply signal, by using a low pass filter, to bias at least one of the MOSFET capacitors.

39. (New) The method of claim 35 in which each of a subset of one or more of the MOSFET capacitors comprises a P-type enhancement mode MOSFET.

40. (New) The method of claim 35 in which each of a subset of one or more of the MOSFET capacitors comprises an N-type depletion mode MOSFET.